Global COE NT IT
CERIES Tohoku University Electro-Related Departments Global COE Program
Center of Education and Research for Information Electronics Systems

Gilbert Multiplier Design

Dr. Vincent Gaudet, Associate Professor
Department of Electrical Engineering
University of Alberta, Canada

Place of Seminar:
1F Laboratory for Brainware Systems, Research Institute of Electrical Communications

The Gilbert multiplier was first introduced in the 1960s, and has since been used in many applications. In this short course, we will look at weak-inversion MOS transistor operation, and how these transistors can be used to design various types of multipliers. We also look briefly at some applications of vector multipliers that process probability mass functions for some communication applications.

Day 1: Weak-inversion MOS transistor modeling June 08, 13:00-16:10

On the first day, transistor I-V models for weak-inversion operation will be introduced. We will look at the impact of VGS, VDS, VT, and transistor size on currents, and how circuits can be designed to operate in weak-inversion. In class, a few small circuits will be presented. In the simulation exercise, students will extract I-V curves from transistors in a 180-nm CMOS technology, using the Spectre simulator. They will then design and simulate a current mirror circuit.

Topics:

- Conventional transistor model
- Weak/Moderate/Strong inversion
- Saturated vs. non-saturated IV curves
- Parasitics
- Transistor size
- Temperature
- Mismatch
- Biasing
- Current mirror example

Design exercise:

- Simulation of IV curves for MOS transistors
- Parameter extraction
- Simulations in process corners
- Simulation of a current mirror Iout vs Iin characteristic curve

Day 2: Translinear principle and circuit analysis June 09, 13:00-16:10

On the second day, we will investigate the translinear principle. Due to the exponential voltage-to-current relationship of weak-inversion MOS transistors, sums of voltages are equivalent to products of currents, simplifying the analysis of weak-inversion circuits. We will go over some hand design examples of a few circuits, leading to the basic four-quadrant weak-inversion CMOS Gilbert multiplier. In the simulation exercise, students will implement these circuits, without being concerned with transistor sizing, mismatch, or speed issues.

Topics:

- Explanation of the Translinear principle
- Example circuits
- Gilbert multiplier example

Design exercise:

- Simulations of a Gilbert multiplier

Day 3: Gilbert Vector Multiplier: Partial product generation
June 10, 13:00-16:10

On the third day, we will continue using translinear analysis to design more complex circuits. Specifically, we will look at a circuit that can generate all partial products of two arbitrarily-large vectors. We will look at both the current-mode and voltage-mode operation of this Gilbert vector multiplier circuit. In the simulation study, students will implement a 4x4 vector multiplier, again not being concerned yet with optimizing the circuit for speed. We will also look at some algorithms in signal processing that require the processing of probability mass functions, and how these computations can be efficiently mapped onto the Gilbert vector multiplier.

Topics:

- Probability propagation problems and why the Gilbert vector multiplier can be used to solve them
- Overview of Gilbert vector multiplier
- Current-mode operation
- Voltage-mode operation
- Design example

Design exercise:

- Design of a 4x4 vector multiplier with partial product generation

Day 4: Gilbert multiplier design: biasing and transistor sizing, Circuit speed and matching
June 11, 13:00-16:10

On the fourth day, we will investigate the optimization of the Gilbert multiplier for speed. We will look at how bias currents can be selected. We will also look at the sources of mismatch in weak-inversion circuits, and why VT mismatch is the most important concern. We will look at techniques to model the impact of mismatch. The simulation study will look at the behaviour of the Gilbert multiplier under various mismatch scenarios.

Topics:

- Choosing a bias current
- Evaluating Speed
- Matching considerations
- Modeling effects of mismatch

Design exercise:

- Simulations of previous day's Gilbert vector multiplier with various mismatch scenarios

Day 5: Low-voltage operation **June 12, 13:00-16:10**

All the previous days, we have assumed weak-inversion transistors that operate in the "saturation" region, implying a large value of VDS. Since this condition can not always be satisfied, especially for low-voltage designs, we will investigate the design of weak-inversion circuits that do not rely on saturated operation. We will design a low-voltage Gilbert multiplier that can operate at supply voltages down to 0.5V. The simulation exercise will involve the design of a 4x4 Gilbert vector multiplier that operates at these low supply voltage values.

Topics:

- Non-saturated operation of weak-inversion transistors
- Impact of non-saturated transistors on multiplier
- Gilbert vector multiplier for low-voltage operation

Design exercise:

- Design of a 4x4 vector multiplier operating at 0.5V supply