CERIES Tohoku University Electro-Related Departments Global COE Program
Center of Education and Research for Information Electronics Systems

2009 International Workshop on New-Concept VLSI Computing and Its Applications

May21-22, 2009
Okinawa Industrial Support Center

Sponsored by:

Center of Education & Research for Information Electronics Systems, Global COE Program of Tohoku University

Scope:

To create future human-oriented information society, advanced intelligent integrated systems which execute autonomously intelligent processing are required. System-on-Chip (SoC) is one of the most important technologies to develop the applications. Investigation of optimal design techniques is essential at all levels such as device, circuit, logic, architecture and application levels. Especially, we focus on the following new paradigm computing related to VLSI :

(1) Interconnection problem
(2) Low-power and energy-efficient architecture
(3) New-concept architecture
(4) System integration methodology for real-world applications

The topics discussed in the Workshop will spawn innovative technologies and develop other technical areas that enrich our ongoing investigation in information and computer engineering.

Program

May 21, 2009

09:10-09:50 Invited Talk 1

Counting Problems and Clones of Functions
Andrei A. Bulatov*, Simon Fraser University, Canada

10:10-12:05: Current-Mode Logic

Robust Multiple-Valued Current-Mode Circuit Components Based on Adaptive Reference-Voltage Control
Naoya Onizawa*, Tohoku University, Japan
Takahiro Hanyu, Tohoku University, Japan

Optimization of Current-Mode MVD-ORNS Arithmetic Circuits
Motoi Inaba*, Tsukuba University of Technology, Japan
Koichi Tanno, University of Miyazaki, Japan
Ryota Sawada, Denso Techno Co., LTD., Japan
Hisashi Tanaka, Miyakonojo National College of Technology, Japan
Hiroki Tamura, University of Miyazaki, Japan

16-Level Current-Mode Multiple-Valued Dynamic Memory with Increased Noise Margin
Golnar Khodabandehloo, University of Windsor, Canada
Mitra Mirhassani*, University of Windsor, Canada
Majid Ahmadi, University of Windsor, Canada

Multiple-Valued Reconfigurable VLSI Processor Based on Superposition of Data and Control Signals
Nobuaki Okada*, Tohoku University, Japan
Michitaka Kameyama, Tohoku University, Japan

Timing-Variation-Aware Multiple-Valued Current-Mode Circuit for a Low-Power Pipelined System
Takashi Matsuura*, Tohoku University, Japan
Hirokatsu Shirahama, Tohoku University, Japan
Masanori Natsui, Tohoku University, Japan
Takahiro Hanyu, Tohoku University, Japan

13:10-14:50: Quantum Logic

Efficient Implementation of Controlled Operations for Multivalued Quantum Logic
David Rosenbaum*, Portland State University, USA
Marek Perkowski, Portland State University, USA

Quantum Finite State Machines as Sequential Quantum Circuits
Martin Lukac*, Portland State University, USA
Marek Perkowski, Portland State University, USA

Synthesis of GF(3) Based Reversible/Quantum Logic Circuits Without Garbage Output
Asif Islam Khan*, UC Berkeley, USA
Md. Mahmud Muntakim Khan, EEE, BUET, Bangladesh
Shuvro Chowdhury , EEE, BUET, Bangladesh
Ayan Kumar Biswas, EEE, BUET, Bangladesh
Masud Hasan, CSE, BUET, Bangladesh

Quantum Realization of Multiple-Valued Feynman and Toffoli Gates Without Ancilla Input
Mozammel H. A. Khan*, East West University, Bangladesh

15:00-15:40 Invited Talk 2

Multi-Valued Modal Fixed Point Logics for Model Checking
Koki Nishizawa*, Tottori University of Environmental Studies, Japan

15:50-17:30: Synthesis of Logic and Digital System

On the Guidance of Reversible Logic Synthesis by Dynamic Variable Reordering
David Y. Feinstein*, Innovations, Inc., USA
Mitchell A. Thornton, Southern Methodist University, USA

Design of a High-Speed Fuzzy Logic Controller Based on Log-Domain Arithmetic
Ali Razib*, University of Alberta, Canada
Scott Dick, University of Alberta, Canada
Vincent Gaudet, University of Alberta, Canada

The Use of Multiple Connected Pseudo Minterms in the Synthesis of MVL Functions
Bambang A. B. Sarif*, CCSE, KFUPM, Saudi Arabia
Mostafa Abd-El-Barr, Department of Information Science, Kuwait University, Kuwait

A Two-Pronged Approach of Power-Aware Voltage Scheduling for Real-Time Task Graphs in Multi-Processor Systems
Naotake Kamiura*, University of Hyogo, Japan
Ayumu Saitoh, University of Hyogo, Japan
Teijiro Isokawa, University of Hyogo, Japan
Nobuyuki Matsui, University of Hyogo, Japan

May 22, 2009

09:30-10:10 Invited Talk 3

Computational Neuroscience and Multiple-Valued Logic
Mitsuo Kawato*, ATR Computational Neuroscience Laboratories, Japan

10:20-12:00: Spectrum Logic

On Periodic Patterns and their Spectra
Claudio Moraga*, European Centre for Soft Computing, Germany
Radomir Stankovic, University of Nis, Serbia
Jaakko T. Astola, Tampere Univ. Technology, Finland

Discrete Hartley Transforms
Claudio Moraga*, European Centre for Soft Computing, Germany

Generating Hard Instances for MaxSAT
Jordi Planes*, Universitat de Lleida, Spain
Felip Manyà, IIIA, CSIC, Spain
Ramon Bejar , Universitat de Lleida, Spain
Alba Cabiscol, DIEI, UDL, Spain

New Encodings from Max-CSP into Partial Max-SAT
Josep Argelich, INESC-ID, Portugal
Alba Cabiscol, DIEI, UDL, Spain
Inês Lynce, IST, INESC-ID, Portugal
Felip Manyà*, IIIA, CSIC, Spain