



CERIES

Tohoku University Electro-Related Departments
Global COE Program

Center of Education and Research for Information Electronics Systems

GCOE Workshop on

Low-Power LSI Technologies and their Application to Mobile Systems

Date: February 27 (Monday), 2012

Site: Conference Room A401, 4F, Laboratory for Nanoelectronics and Spintronics,
Research Institute of Electrical Communication, Tohoku University
(2-1-1 Katahira, Aoba-ku, Sendai 980-8577, JAPAN)

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“Center of Education and Research for Information Electronics Systems”

Program:

1. 13:30 - 14:00

Lecturer: **Prof. Vincent C. Gaudet** (University of Waterloo, Canada)

Title: **Low-Power and High-Speed Approaches to LDPC and Turbo Decoding**

Author: V. Gaudet, N. Onizawa, and T. Hanyu

Abstract:

This talk will review high-performance VLSI architectures to decode capacity-approaching error-control codes such as Turbo and Low-Density Parity-Check codes. We will review the sum-product algorithm and its variants, as well as recent stochastic decoding techniques. VLSI architectural aspects will be discussed, including issues with parallel and bit-serial implementations. Recent approaches for high-performance decoding will be reviewed, including high-speed and low-power techniques.

2. 14:00 - 14:30

Lecturer: **Tatsunori Obara**(ECEI, Tohoku University)

Title: **Joint MMSE-FDE & spectrum combining for single-carrier transmission**

Author: T. Obara and F.Adachi

Abstract:

Minimum mean square error frequency-domain equalization (MMSE-FDE) is a promising equalization technique for the broadband single-carrier (SC) transmission. However, the presence of timing offset produces the inter-symbol interference (ISI) and degrades the bit error rate (BER) performance. In this paper, we present joint MMSE-FDE & spectrum combining which can achieve the frequency diversity gain while suppressing the negative impact of timing offset for the SC transmission.

3. 14:30 - 15:00

Lecturer: **Dr. Naoya Onizawa** (University of Waterloo, Canada)

Title: **Asynchronous and Clockless Stochastic Decoding of LDPC Codes**

Author: N. Onizawa, W. J. Gross, T. Hanyu, and V. C. Gaudet

Abstract:

This talk introduces asynchronous and clockless stochastic computation for low-power and high-speed low-density parity-check (LDPC) decoding. Clockless stochastic decoding could provide low-complexity hardware without clocking, lowering power dissipation, but it would potentially have some issues: metastability and lock-up that stops decoding before its convergence. We model the timing behaviours to investigate bit-error performance of clockless decoding. The timing model is developed using transistor-level simulation results in TSMC 90-nm CMOS technology. Based on the model, we show how two issues affect bit-error performance and compare the performance with the sum-product algorithm and synchronous stochastic decoding.

4. 15:00 -15:30

Lecturer: **Atsushi Matsumoto**(RIEC, Tohoku University)

Title: **Fine-grained power-gating scheme for an asynchronous integrated circuit**

Author: A. Matsumoto, T. Kawano and T. Hanyu

Abstract:

In this talk, we shows the fine-grained power-gating scheme based on sharing asynchronous control signals. Because the local handshaking control signals in the asynchronous controller are also used as the power-switch control signal, power gating controller is realized by a simple logic gate per each pipeline stage. By applying the proposed fine-grained power gating scheme to an asynchronous pipeline circuit, leakage current in idle state is greatly reduced with low hardware and latency overhead. Simple circuits designed with ASPLA 90-nm CMOS technology are simulated and the results are compared with ones of circuits without power-gating scheme.

15:30 - 15:45 Break

5. 15:45 - 16:15

Lecturer: **Tetsuya Yamamoto** (ECEI, Tohoku University)

Title: **Complexity Reduced Near ML Block Detection for Single-Carrier MIMO Spatial Multiplexing**

Author: T. Yamamoto and F. Adachi

Abstract:

For high-speed packet access, multiple-input multiple-output (MIMO) spatial multiplexing are indispensable techniques. Single-carrier (SC) MIMO spatial multiplexing has been gaining an increasing popularity especially in uplink communications (mobile terminal-to-base station) because of its lower peak-to-average power ratio (PAPR) property. However, SC-MIMO spatial multiplexing must deal not only with inter-antenna interference (IAI) but also with inter-symbol interference (ISI) caused by multi-path propagation, and therefore, a powerful signal detection scheme should be designed. The use of maximum likelihood (ML) detection, which is an optimum detection scheme, is not realistic due to its extremely high detection complexity. In this talk, we will present our recent work on the complexity reduced near ML detection.

6. 16:15 - 16:45

Lecturer: **Shoun Matsunaga** (CSIS, Tohoku University)

Title: **Nonvolatile TCAM Using MTJ-Based Logic-in-Memory Architecture and Its Future Prospects**

Author: S. Matsunaga and T. Hanyu

Abstract:

Ternary content-addressable memories (TCAMs) are attractive hardware with the high-speed fully-parallel data search, which are useful for IP-packet classification in routers, and virus-pattern matching in mobile devices. However, the conventional CMOS-based TCAM has two major issues; increasing standby power and high bit-cell cost.

We present novel nonvolatile fully parallel TCAM for realizing compactness and low power consumption. The use of magnetic tunnel junction (MTJ)-device-based logic-in-memory architecture realizes both compactness of cell size and ultra-low standby power consumption. Moreover, a match-line segmentation scheme is also utilized to reduce active power consumption, which results in low search energy of the proposed TCAM.

As a future prospect, it is also useful to apply the MTJ-based logic-in-memory architecture to a high-performance and a low-power memory-based computational VLSI system.

7. 16:45 - 17:15 :

Lecturer: **Daisuke Suzuki** (CSIS, Tohoku University)

Title: **Nonvolatile Field-Programmable Gate Array Using an MTJ/MOS-Hybrid Structure and Its Future Prospect**

Author: D. Suzuki and T. Hanyu

Abstract:

A logic element (LE) using a magnetic-tunnel-junction (MTJ) and MOS-hybrid structure is presented for a standby-power-free nonvolatile field-programmable gate array (NV-FPGA). Since the current level of a selector tree together with MTJ devices is directly evaluated and amplified by a differential sense amplifier in the lookup-table circuit, the number of wasted sense amplifiers is greatly reduced. Moreover, the use of dynamic current-mode logic based circuitry makes it possible a high-speed operation with low-active power dissipation due to the elimination of steady current-path. The usefulness of the proposed LE is demonstrated and the future prospects for the NV-FPGA are also discussed.

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