CERIES Tohoku University Electro-Related Departments Global COE Program
Center of Education and Research for Information Electronics Systems

Short Course on Power Management for Mobile Devices

February 1 to 5, 13:00 ~ 16:10
1F, Laboratory for Brainware Systems, RIEC, Tohoku University

Wai Tung Ng

Professor, Associate Chair, Undergraduate Studies

University of Toronto

Department of Electrical and Computer Engineering

10 King's College Road, Toronto ON, Canada M5S 3G4

Tel: (416) 978-6249
Email: ngwt@vrg.utoronto.ca
Web: www.vrg.utoronto.ca/~ngwt

Course Description

Power management, especially for battery power portable electronics has became an important enabling technology in the last few years. There are many approaches to managing and saving power consumption. For example, there are many reported techniques, ranging from using software strategies to minimize circuit switching activities, dynamic voltage scaling that adjusts supply voltage and clock frequency, and the used of multiple threshold devices to reduce power consumption for non-critical path circuits, etc. However, an important link that is often neglected in power management is the design of high efficiency switching power supplies. In this short course, we will focus on the design and implementation of integrated DC-DC converters that serve as an essential component in all power management systems.

With the increasing needs to incorporate more complex mixed-signal controller for switched mode power supplies, CMOS compatibility becomes a very important consideration in monolithic Smart Power ICs. Designers need to examine various design considerations for the implementation of integrated DC-DC converters, which include switched mode power supply topology, digital vs. analog controller, power conversion efficiency, dead-times, choice of components, and power transistors for the output stages. In particular, EDMOS device structures, fabrication techniques and compatibility issues with CMOS process must be considered. Key device characteristics such as ruggedness, on-resistance, gate capacitance, switching speed and layout strategies are required for optimum power conversion efficiencies. Recent research work on integrated DC-DC converters with novel features such as segment output stage, digital spread spectrum for EMI suppression, dead-time control will be discussed. The benefit of the segmented output stage via a true power management system for portable audio applications will also be demonstrated

This short course will show a systematic approach to the design and integration of digitally controlled switch-mode power supplies (SMPS) for DC-DC converters. It is expected that the audience attending this course has knowledge about basic switching converter topologies and understands fundamentals of conventional feedback control theory.

The seminar will consist of three main parts that cover the design and implementation of a complete SMPS, including detailed explanation of digital controller, power stage, and gate drivers.

1. Low Power Digital Controllers

The first part of the course, will show basic digital control structures and address problems of their high-power consumption, quantization effects, and large on-chip area. Specifically, difficulties in the design of basic functional blocks, such as, analog-to-digital converter (ADC), compensator, digital pulse-width modulator (DPWM), and current sensing circuits will be addressed. We will then introduce different architectures for each of these blocks that have low current consumption, fast processing time, and occupy small on-chip area. A survey of ADC architectures will include flash converters, delay-line and ring oscillator-based structures, as well as programmable ADCs. Compensators will be presented through conventional PID and nonlinear multi-mode structures. Delay line, hybrid, segmented, and segmented-ring DPWM architectures will also be described and their characteristics assessed.

2. Output Power stages and Integration Issues

This part begins with a review of smart power integrated circuit technology. This includes a survey of current power devices, fabrication processes, integration issues and existing applications. Problems related to the realization of power transistors and gate drivers in latest deep submicron technologies will be addressed. Accordingly, guidelines for effective power MOSFETs design in deep submicron technologies will be given. Special attention will be given to design challenges such as device layout, isolation techniques, limitations on power and thermal dissipation, gate drive circuits and output stage segmentation. We will also talk about effective IC packaging and integration with micro-inductors and capacitors.

3. Output Power stages and Integration Issues

In this section, we will demonstrate design principles and showcase potential advantages of digital control. We will show a step-by-step implementation of two digitally controlled SMPS. First is a current-mode controlled 10 MHz converter with a segmented power stage. The second example will show a multi-mode digital power management IC consisting of dual-mode controller and high frequency power stage. At heavy loads the dual-mode controller operates as PWM regulator, while, when the load is light it performs digital pulse-frequency modulation. In addition, the concept of using digital spread spectrum to suppress EMI will also be demonstrated.

We expect that, after attending the seminar, the audience will obtain a useful insight into problems related to monolithic integration of digital controlled SMPS and gain understanding of basic design principles used in their practical realization.

Course Outline

Part I: Integrated Digital Controllers for high-frequency DC-DC SMPS

- Review of basic digital control architectures
  - Digital PWM controller and its analog equivalent
  - Current program mode controllers
  - All-digital implementation
  - Mixed-signal digital controllers
- Implementation problems
  - High-frequency high-resolution requirements and sources of power losses
  - Quantization effects
  - Design optimization of digital pulse-width modulated converters
  - Minimal hardware requirements for ADC, Compensator and DPWM
- A review of basic functional blocks architectures
  - ADC architectures
  - Flash converter
- Windowed flash
- ADCs with non-uniform quantization steps
  - Delay-line and ring oscillator based structures
  - ADC with programmable reference
  - Compensator Implementations
  - PID compensator
  - High-order structures
  - Non-linear multi-mode compensators
  - A review of DPWM Architectures and their limitations
  - Hybrid architectures
  - Segmented DPWM
  - Segmented ring
  - Sigma-delta and dithering structures
- Design optimization of digital current program mode controllers
  - Current sensing (sense FET topology and wide bandwidth amplifier)
  - Multi-mode current sense circuits and all digital implementation

Part II: Power Stage Integration

- ☐ Integrated Power Devices
- ☐ Device performance and trade-off parameters
  - ■ MOSFET vs. Bipolar Power Transistors
  - ■ Breakdown Voltage
  - ■ Ron, Gate Charge, FOM
- ☐ Isolation Techniques
  - ■ Self isolation
  - ■ Junction Isolation
  - ■ Dielectric Isolation
- ☐ Smart Power IC Processing Technologies
  - ■ HVCMOS
  - ■ BCD
- ☐ Smart PIC Output Drivers
  - ■ Half bridge
  - ■ H-bridge
  - ■ gate drive circuits, level shifters
- ☐ Packaging
  - ■ Die Attachment
  - ■ Wire Bonding
  - ■ High Pin-count Packages
- ☐ Smart PIC Applications
  - ■ Display drivers
  - ■ Motor Drive
  - ■ DC-DC converters
- ☐ Design Flow, CAD Tools

Part III: Design Examples

- ☐ 10 MHz Digital Current Program-Mode SMPS IC With Segmented Switches
- ☐ Multi-Mode DPWM/DPFM Controlled DC-DC Converter with digital spread spectrum EMI reduction
- ☐ A power management system for class D digital audio application

Presenter's Biography and Contact Information

Wai Tung Ng (M'90, SM'04) received his B.A.Sc., M.A.Sc. and Ph.D. degrees in Electrical Engineering from the University of Toronto, in 1983, 1985 and 1990, respectively. His graduate research work focused on analog integrated circuits design and smart power integrated fabrication processes. In 1990, Dr. Ng joined the Semiconductor Process and Development Center of Texas Instruments, Dallas TX, to work on LDMOS power transistors for automotive applications. His academic career started in 1992 when he joined the Department of Electrical and Electronic Engineering, at the University of Hong Kong. Dr. Ng joined the University of Toronto in 1993. He was promoted to associate professor in 1998 and full professor in 2008. His research interests cover a wide spectrum, ranging from advanced MOS and RF BJT device designs to analog circuits. He has published extensively in the areas of VLSI power management circuits, integrated DC-DC converters, smart power integrated circuits, power semiconductor devices and fabrication processes. His most notable recent contribution is to improve the power conversion efficiency and transient response in digitally controlled low power DC-DC converters for portable electronics. Prof. Ng is also serving at the chair of the IEEE Toronto Section (2010-2011).